DERWENT-ACC-NO: 1991-019969

DERWENT-WEEK: 199103

TITLE: Gate structure for MOSFEt - includes silicon-rich oxide buffer layer between gate insulation and gate electrode

PATENT-ASSIGNEE: ANONYMOUS[ANON]

PRIORITY-DATA: 1990RD-0320069 (November 20, 1990)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
RD 320069 A	December 10, 1990	N/A	000	N/A

INT-CL (IPC): H01L000/01

ABSTRACTED-PUB-NO: RD 320069A

BASIC-ABSTRACT:

An a MOSFET device, an Si-rich oxide layer (16) is interposed between gate insulation layer (14) and metal (silicide) gate electrode layer (18).

ADVANTAGE - The intermediate layer serves as a buffer between the gate insulation and gate electrode and minimises degradation of the insulation layer by the metal (silicide), without affecting threshold voltage; enhancement or depletion mode FETs can be made without channel implantation and in partic. a depletion mode device operating at low temp. can be fabricated

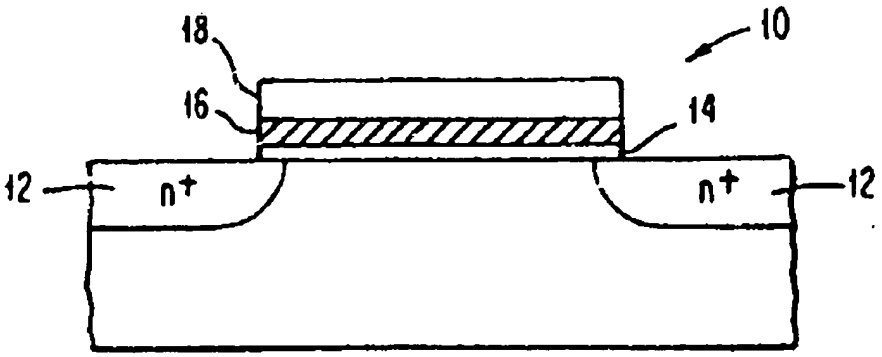
TITLE-TERMS: GATE STRUCTURE MOSFET SILICON RICH OXIDE BUFFER LAYER GATE INSULATE GATE ELECTRODE

DERWENT-CLASS: L03 U12

CPI-CODES: L04-C11C; L04-C12A; L04-E01B1;

EPI-CODES: U12-D02A; U12-E02;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1991-008766
Non-CPI Secondary Accession Numbers: N1991-015199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